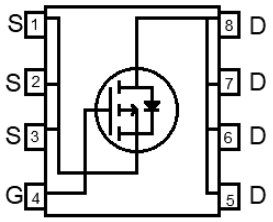
-60V P-Channel Power MOSFET

• General Description

It combines trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$.

• Product Summary



V_{DS}= -60V

$R_{DS(ON)}$ = 23mΩ

I_D= -26A

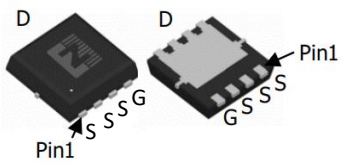
• Features

■AEC-Q101 Qualified

■Low $R_{DS(ON)}$ to minimize conductive loss

■High GOX reliability

■Low Thermal resistance



DFN3*3

•Application

■BLDC Motor driver

■DC-DC

■Load Switch

•Ordering Information:

Part NO.	ZMA230P06M
Marking	230P06
Packing Information	REEL TAPE
Basic ordering unit (pcs)	5000

•Absolute Maximum Ratings (T_C=25℃)

Parameter	Symbol	Conditions	Value	Unit
Drain-Source Voltage	V_{DS}		-60	V
Gate-Source Voltage①	V_{GS}		±20	V
Continuous Drain Current	I_D	T_C=25℃	-26	A
	I_D	T_C=75℃	-23	A
	I_D	T_C=100℃	-20	A
Pulsed Drain Current	I_{DM}	Pulsed; t_p ≤ 10 μs; T_{mb} = 25 °C;	-104	A
Total Power Dissipation	P_D	T_C=25℃	56	W
Total Power Dissipation	P_D	T_A=25℃	2.5	W
Operating Junction Temperature	T_J		-55 to +175	℃
Storage Temperature	T_{STG}		-55 to +175	℃
Single Pulse Avalanche Energy	E_{AS}	L=0.1mH, V_{GS}=-10V, Rg=25Ω,	45	mJ
		L=0.5mH, V_{GS}=-10V, Rg=25Ω,	94.5	mJ
ESD Level (HBM)	CLASS 2			

●Thermal resistance

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance, junction - case	R_{thJC}		-	2.7	°C/W
Thermal resistance, junction-ambient②	R_{thJA}		-	60	°C/W
Soldering temperature	Tsold		-	260	°C

●Electronic Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} =0V, I_D =-250uA	-60			V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} =V_{DS}, I_D =-250uA	-1.3	-1.8	-2.5	V
Drain-Source Leakage Current	I_{DSS}	V_{GS}=0V, V_{DS}= -60V			1.0	uA
Gate- Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS} = 0V			100	nA
Static Drain-source On Resistance	$R_{DS(ON)}$	V_{GS}=-10V, I_D= -15A		23	34	mΩ
		V_{GS}=-4.5V, I_D= -10A		29	41	mΩ
Forward Transconductance	g_{FS}	V_{DS} =-5V, I_{SD} = -10A		20		s
Diode Forward Voltage	V_{FSD}	V_{GS} =0V, I_{SD} = -15A			1.3	V

●Dynamic characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input capacitance	Ciss	f = 1MHz, V_{DS}=-25V	-	3300	-	pF
Output capacitance	Coss		-	148	-	
Reverse transfer capacitance	Crss		-	96	-	
Gate Risistance	Rg	f = 1MHz	-	8		Ω
Total gate charge	Qg	V_{DD} = -15V, I_D = -10A, V_{GS} = -10V	-	46	-	nC
	Qg(-4.5v)		-	21	-	
Gate - Source charge	Qgs		-	6.3	-	
Gate - Drain charge	Qgd		-	8.6	-	
Turn-ON Delay time	$t_{D(on)}$	V_{GS}=-10V,V_{DS}=-15V, R_G =3.3Ω, I_D =-10A	-	13	-	ns
Turn-ON Rise time	t_r		-	21	-	ns
Turn-Off Delay time	$t_{D(off)}$		-	87	-	ns
Turn-Off Fall time	t_f		-	34	-	ns
Reverse Recovery Time	t_{RR}	V_{DD}=-20V, dI_S/dt = 100A/us, I_S=-20A	-	66	-	ns
Reverse Recovery Charge	Q_{RR}		-	263	-	nC

Fig.1 Gate-Charge Characteristics

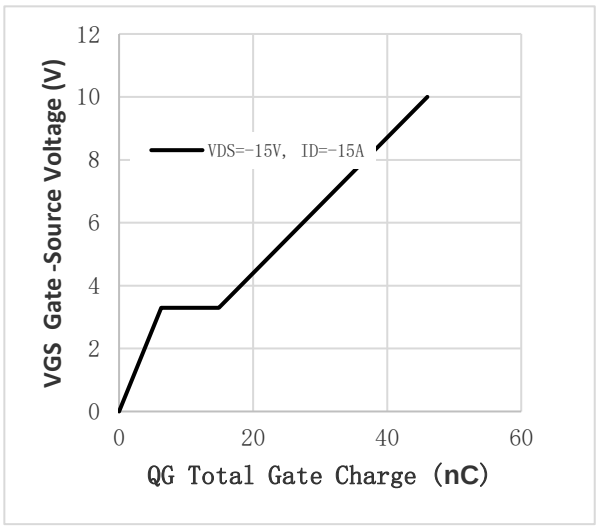


Fig.2 Capacitance Characteristics

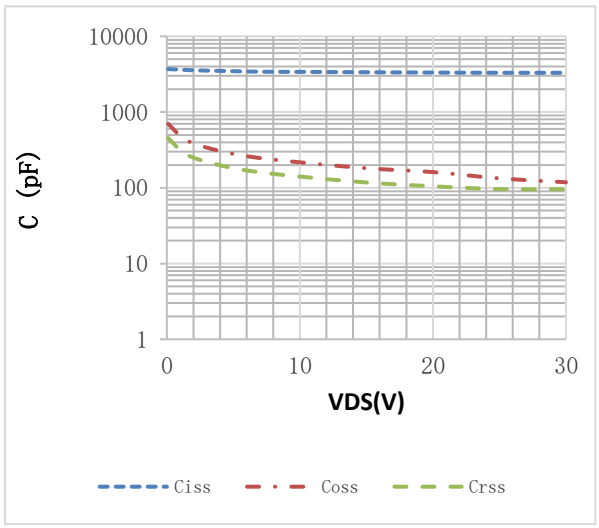


Fig.3 Power Dissipation

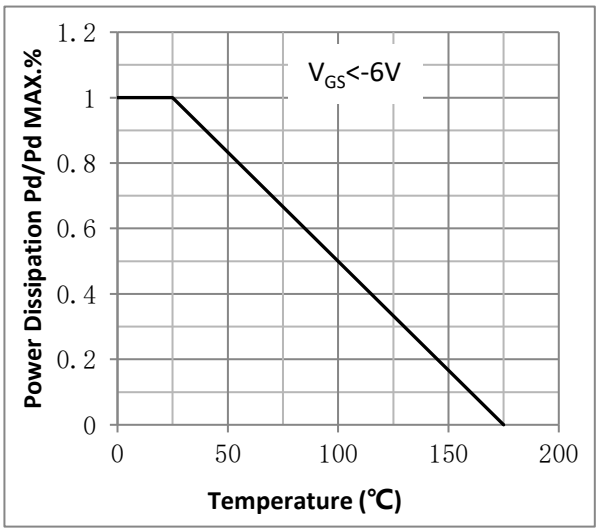


Fig.4 Typical output Characteristics

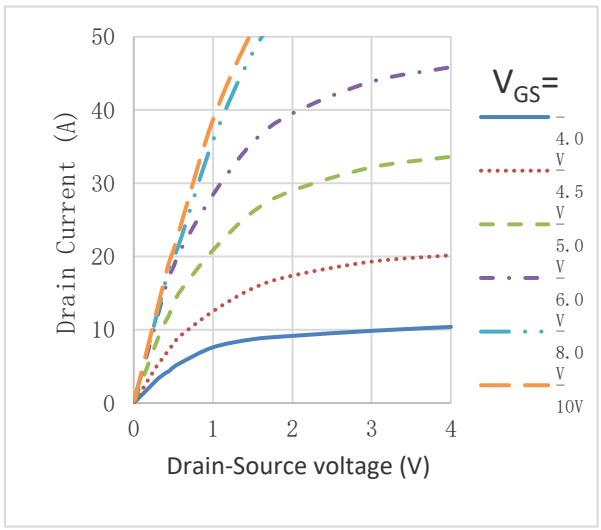


Fig.5 Threshold Voltage V.S Junction Temperature

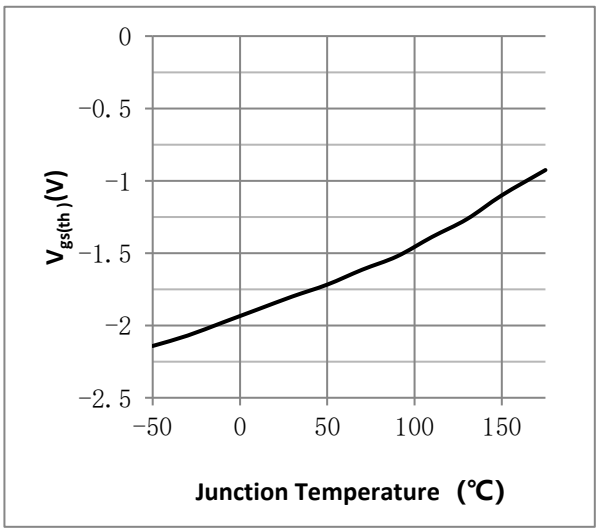


Fig.6 Resistance V.S Drain Current

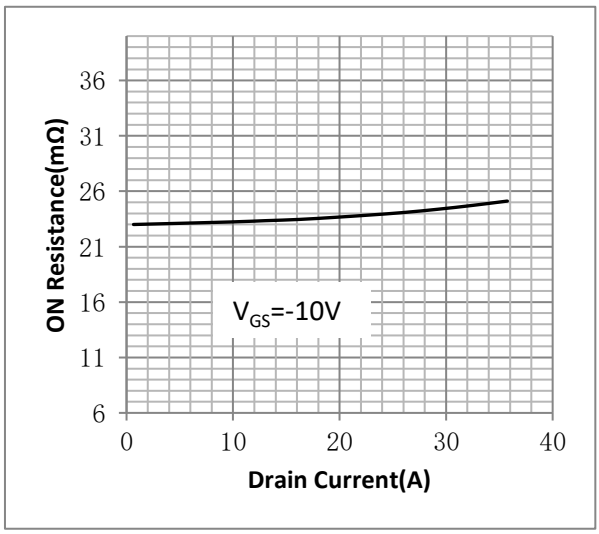


Fig.7 On-Resistance VS Gate Source Voltage

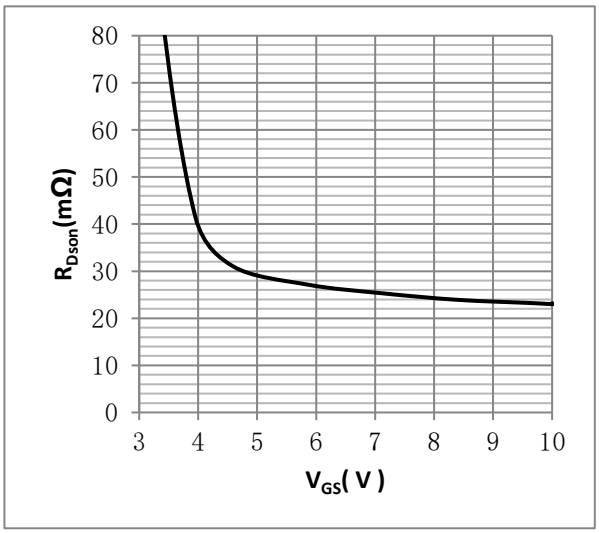


Fig.8 On-Resistance V.S Junction Temperature

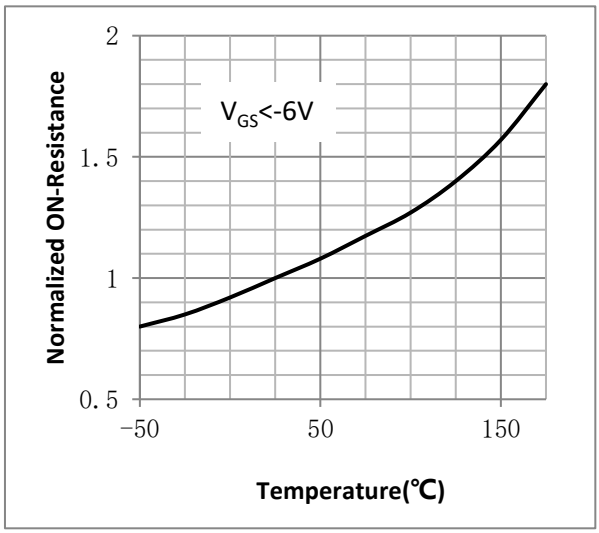


Figure 9. Diode Forward Voltage vs. Current

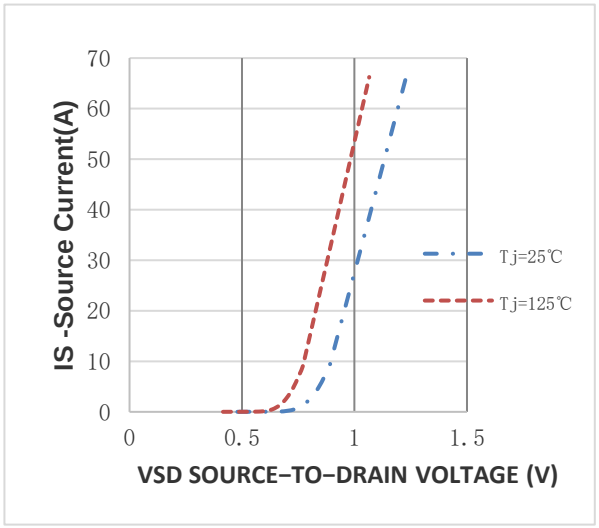


Figure 10. Transfer Characteristics

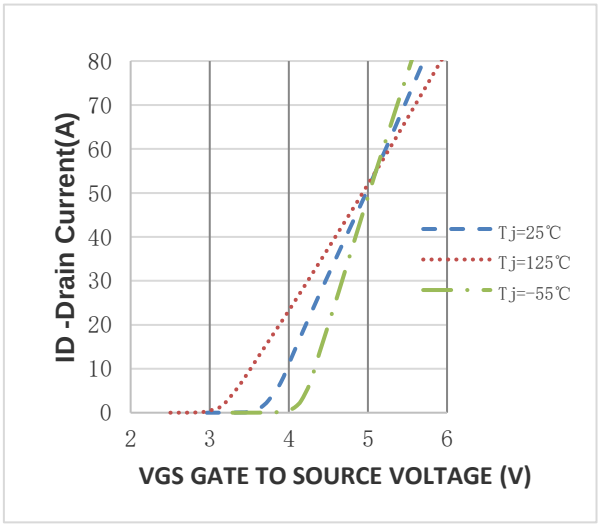


Fig.11 Safe Operating Area

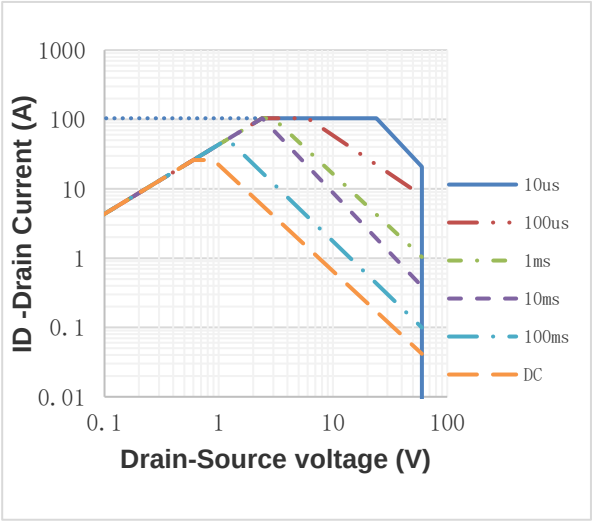
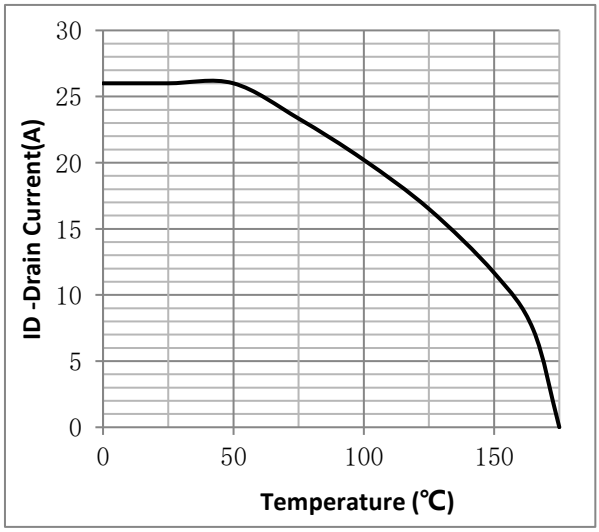
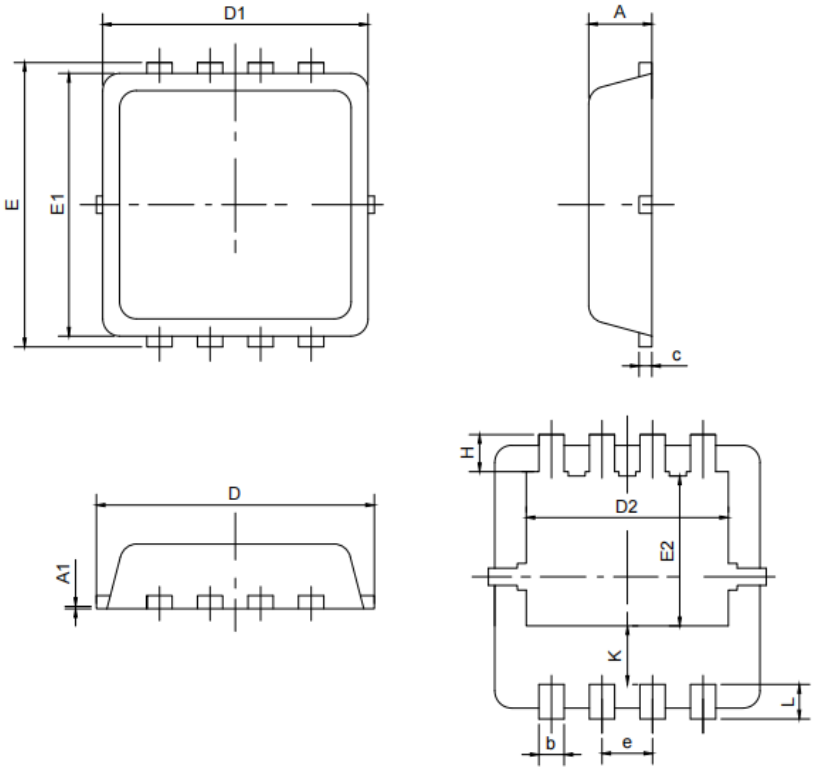


Fig.12 ID vs. Case Temperature③

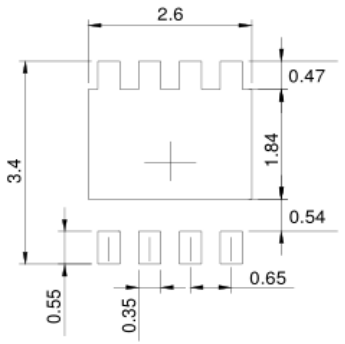


●DFN3*3 Package Outline



SYMBOLS	COMMON	
	MM	
	MIN.	MAX.
A	0.70	0.85
A1	0.00	0.05
b	0.20	0.40
c	0.10	0.25
D	3.00	3.45
D1	3.00	3.25
D2	2.29	2.65
E	3.15	3.45
E1	2.90	3.20
E2	1.32	1.98
e	0.55	0.75
H	0.28	0.65
K	0.59	1.13
L	0.30	0.50

RECOMMENDED LAND PATTERN



UNIT: mm

Note:

① Pulse : VGS=+20V/-20V, Duty cycle=50%,Tj=175℃, t=1000 hours; For DC， the following test conditions can be passed: VGS=-20V/+10V, Tj=175℃, t=1000 hours；

② Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate；

③Practically the current will be limited by PCB, thermal design and operating temperature. VGS=-10V.

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Revision History

Version	Date	Change
A	2021.2.3	
B	2022.9.7	1.Add Reach,HF figure,2.ID modify
C	2023.12.8	Correct package outline dimension